CS311 - Computer Architecture - Spring 2017
Homework 8 – 105 points
Due: May 5

1. (15 points) Exercise 5.3.3, pg. 550, and make the following changes to the problem

   - use the following set of memory references: 6, 214, 175, 214, 6, 84, 65, 174, 64, 105, 85, 215, 104, 213.
   - change the cache size for each cache to 16 words.

   You may deal solely with word addresses for this problem (i.e., there's no need to convert them to byte addresses). For each of the memory references, specify the cache index, tag value and whether it results in a hit or miss.

2. (5 points) Exercises 5.4.1–5.4.3, pg. 551. Use the following address bits: Tag: 31-13; Index: 12-4; Offset: 3-0. You should assume that we are using word addressing. FYI: A cache line is synonymous with a cache block.

3. (10 points) Exercises 5.7.1–5.7.3, pg. 554. Use the following values for size, miss rate and hit time:

	L1 size	L1 miss rate	L1 hit time
P1	1 KB	11.4%	0.96ns
P2	2 KB	8.0%	1.08ns

   Give you answers in 5.7.2 in units of clock cycles, and assume in 5.7.3 that the miss rates listed are only for memory accesses and that instruction accesses have a 0% miss rate.

4. (10 points) Exercises 5.8.1–5.8.3, pg. 555. Use the same modified list of memory references as you used in Problem 1.

5. (10 points) Exercises 5.8.4, 5.8.5, pp. 555, 556. Use the following values in place of the values for scenarios a and b: 1.5, 4GHz, 110ns, 4.5%, 10 cycles, 2.5%, 20 cycles and 1.5%.

6. (15 points) Consider three processors with different cache configurations:

   Cache 1 : direct-mapped with one-word blocks

   Cache 2 : direct-mapped with four-word blocks

   Cache 3 : two-way set associative with four-word blocks

   The following miss rate measurements have been taken:

   Cache 1 : Instruction miss rate 4%; data miss rate 6%.

   Cache 2 : Instruction miss rate 2%; data miss rate 4%.

   Cache 3 : Instruction miss rate 2%; data miss rate 3%.

   For these processors, one-half of the instructions contain a data reference. Assume that the cache miss penalty is 6 + (block size in words). The CPI for this workload was measured on a processor with cache 1 to be 2.0

   (a) Determine which processor spends the most cycles on cache misses.

   (b) Assume the cycle time for processors 1 and 2 is 420 ps and the cycle time for processor 3 is 310 ps. Determine which processor is the fastest and which is the slowest.

(over)

7. (10 points) Consider a virtual memory system with the following properties:

   - 40-bit virtual byte address
   - 16 KB pages
   - 36-bit physical byte address

   (a) What is the total size of the page table, assuming that the valid, protection, dirty and use bits take a total of 4 bits and that all the virtual pages are in use? You may assume that the disk addresses are not stored in the table.

   (b) Assume that this system uses a two-way set associative TLB with a total of 256 translations. Show the virtual-to-physical mapping with a figure like the top part of Figure 5.24 on page 505. Make sure to label the width of all fields and signals.

8. (10 points) Exercises 5.10.1,5.10.2, pg. 557, 558. Use the following sequence of memory references: 48310, 8204, 32110, 20186, 43696, 20390, 32308, 28568. If you need to bring in new pages from secondary memory, use a physical page number of 13 for the first, 14 for the next, and so on.

9. (20 points) Assume that we have the following page references:

   1, 2, 3, 4, 3, 2, 5, 2, 6, 7, 8, 5, 6, 9

   and we can only fit four pages in main memory. Determine the number of page faults for each of the following strategies, and show which pages are in memory every time there is a change. Also, specify which, if any, of these methods are optimal for this set of page references. Note: for the NFU schemes, assume the time interval where counters are incremented is a single cycle (i.e., every reference adds one to the counter).

   (a) LRU

   (b) FIFO

   (c) Clock

   (d) NFU with no erasure of reference bits

   (e) NFU with erasure of reference bits after every 5th page reference

   (f) Tree-PLRU